CLAIMS

What is claimed is:

1.   An apparatus comprising:
a host controller; and
a host controller driver,
wherein a plurality of banks containing a plurality of queue element transfer descriptors (qTDs) are created for a plurality of buffers posted to the host controller driver, and the qTDs are circularly linked.

2.   The apparatus of claim 1, wherein the host controller is an enhanced host controller interface (EHCI) host controller.

3.   The apparatus of claim 1, wherein the banks are associated with a particular buffer in the plurality of buffers.

4.   The apparatus of claim 3, wherein the plurality of buffers are ordered in an incremented order.

5.   The apparatus of claim 4, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

6.   The apparatus of claim 1, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.

7.   An apparatus comprising:
a host controller; and
a host controller driver coupled to the host controller,
wherein the host controller arranges queue element transfer descriptors (qTDs) in a circularly linked order.

8.   The apparatus of claim 7, wherein a plurality of banks containing a plurality of qTDs are created for a plurality of buffers posted to the host controller driver.

9.   The apparatus of claim 7, wherein the host controller is an enhanced host controller interface (EHCI) host controller.

10.   The apparatus of claim 8, wherein the banks are associated with a particular buffer in the plurality of buffers.

11.   The apparatus of claim 10, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

12.   The apparatus of claim 8, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.

13.   A system comprising:
a bus;
a first host controller coupled to the bus; and
a second host controller coupled to the first host controller;
wherein the first host controller arranges queue element transfer descriptors (qTDs) in a circularly linked order.

14.   The system of claim 13, wherein a plurality of banks containing a plurality of qTDs are created for a plurality of buffers posted to a host controller driver.

15.   The system of claim 13, wherein the first host controller is an enhanced host controller interface (EHCI) host controller.

16.   The system of claim 14, wherein the banks are associated with a particular buffer in the plurality of buffers.

17.   The system of claim 16, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

18.   The system of claim 13, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.